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Color Supplement to NIST Special Publication 400-93: *Semiconductor Measurement Technology*: Design and Testing Guides for the CMOS and Lateral Bipolar-on-SOI Test Library

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Semiconductor Measurement Technology:
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Abstract

This report is the supplement to the NIST Special Publication entitled "*Semiconductor Measurement Technology:* Design and Testing Guides for the CMOS and Lateral Bipolar-on-SOI Test Library." This supplement contains the complete set of figures from the above-mentioned document with the test structures provided in color for easier interpretation.

Key words: bipolar; CAD; CMOS; Magic; NIST8; NIST9; SOI; technology file; test chip; test structure

Introduction

This report is the supplement to the design and testing guide [1] for the test library from which test chip NIST8 and test wafer NIST9 were derived. (This supplement contains the complete color set of figures from the NIST Special Publication.) The test library, NIST8, and NIST9 were designed for process monitoring and device parameter extraction to evaluate and compare CMOS (Complementary Metal-Oxide-Semiconductor) test structures, including devices and circuits, fabricated on both bulk silicon and SOI (Silicon-on-Insulator), specifically SIMOX (Separation by the IMplantation of OXygen), wafers. The test library consists of both CMOS-on-SOI and lateral bipolar-on-SOI modules. From it, 20 modules were assembled to create the CMOS test chip NIST8 that was fabricated using a standard bulk CMOS foundry through the MOSIS [2] service. Also, the SOI/SIMOX test wafer NIST9 was assembled from modules contained in this test library. NIST9 contains approximately 1000 modules, and 14 processing masks are used to realize depletion-mode MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors), lateral bipolar devices,

and CMOS MOSFETs with source-to-channel ties. The SOI/SIMOX "technology file" used with the CAD graphic layout editor Magic* [3] was modified to include the layers necessary to realize these 14 masks.

From the test library, a variety of modules can be assembled to create a new test chip or test wafer, or the modules can be used as "drop-in's." The NIST Special Publication [1] explains the philosophy behind the module sizes, dimensions, placements, nomenclature, architecture, and so forth. Each one of the modules described is designed to facilitate packaging.

NIST8 is the CMOS test chip that was assembled from 20 modules in the test library. It is a CMOS-on-SOI design converted to a CMOS on bulk silicon design via the technology file.

The SOI/SIMOX test wafer, NIST9, is also described in the NIST Special Publication. It describes its formation, organization, and the test structures that were included from the test library. The processing modules which include the alignment marks were strategically placed to ease the task of mask alignment. To study parameter variations across NIST9 a test module was designed and placed such that comprehensive data can be obtained for process evaluation.

For information on obtaining the test library, NIST8, NIST9, and the SOI/SIMOX technology file, please contact:

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This author can also be contacted for the NIST Special Publication of which this is the color supplement.

Acknowledgments

We would like to thank Jane Walters for her expert guidance in making this report a reality.

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* In this report, commercial equipment, instruments, and computer programs are identified to specify the procedure adequately. This does not imply recommendation or endorsement by NIST, nor does it imply that the equipment or program is the best available for the purpose. In spite of the authors' experiences that the programs perform correctly on every set of data which has been tried, there can be no assurance that the program will perform equally well on all (possibly anomalous) data. Therefore, both the authors and NIST assume no liability for possible losses resulting from the use of these programs.

References

1. Marshall, J. C. and Zaghloul, M. E., *Semiconductor Measurement Technology:* Design and Testing Guides for the CMOS and Lateral Bipolar-on-SOI Test Library, NIST Special Publication 400-93 (March 1994).

2. Richardson, L., et al., MOSIS User Manual, University of Southern California (1988).

3. Scott, W., Mayo, R., Hamachi, G., and Ousterhout, J., 1986 VLSI Tools: Still More Works by the Original Artists, Computer Science Division (EECS), Univ. of California, Berkeley, CA, Report No. UCB/CSD 86/272 (December 1985).

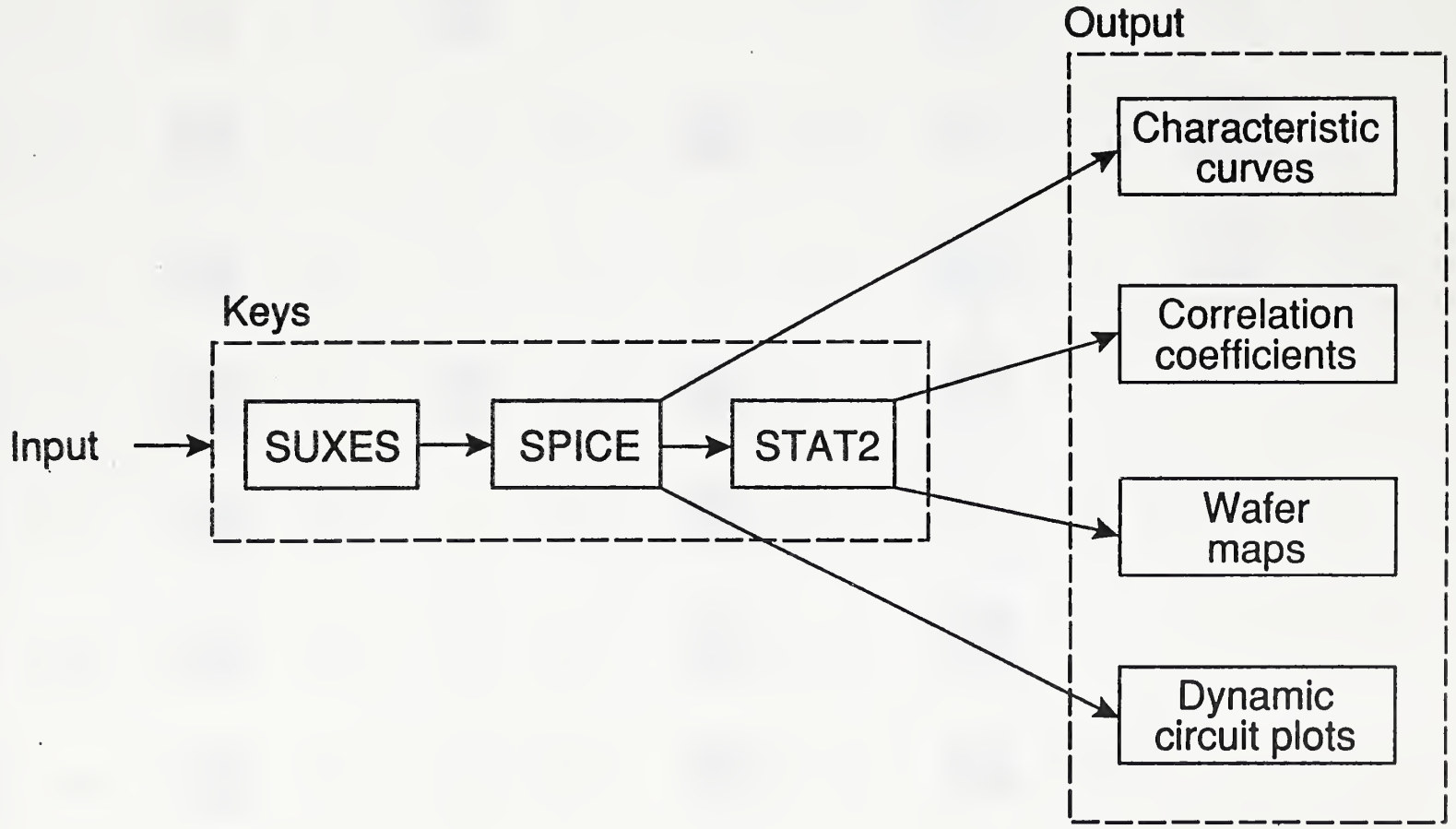

Figure 1. Simplified block diagram for the computer procedure KEYS.

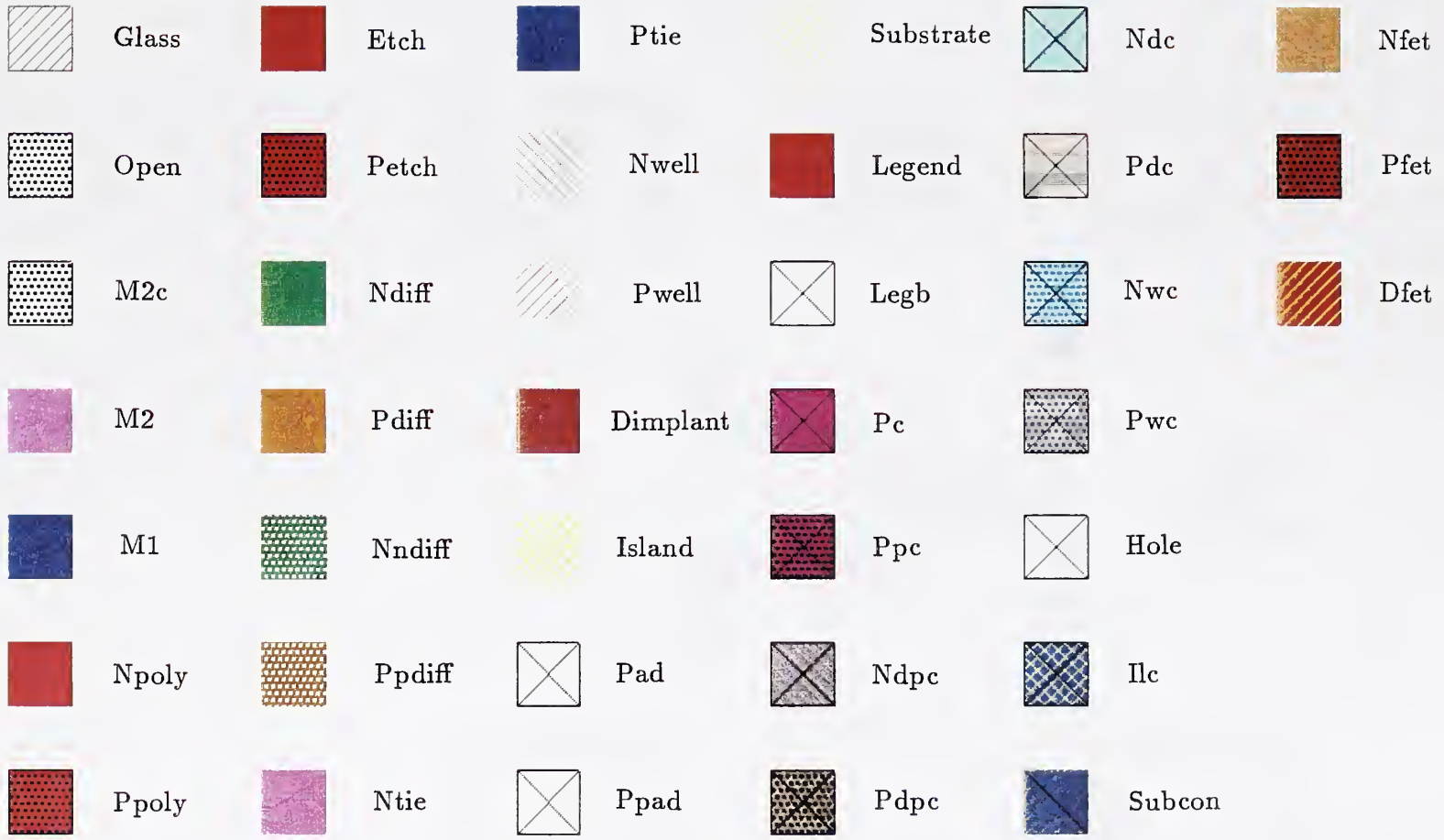

Figure 2. Key to the shading in the figures. These layers correspond to the Magic layers in the SOI/SIMOX technology file.

Figure 3. *P*-channel MOSFET found in the test library, NIST8, and NIST9.

Figure 4. *N*-channel MOSFET found in the test library, NIST8, and NIST9.

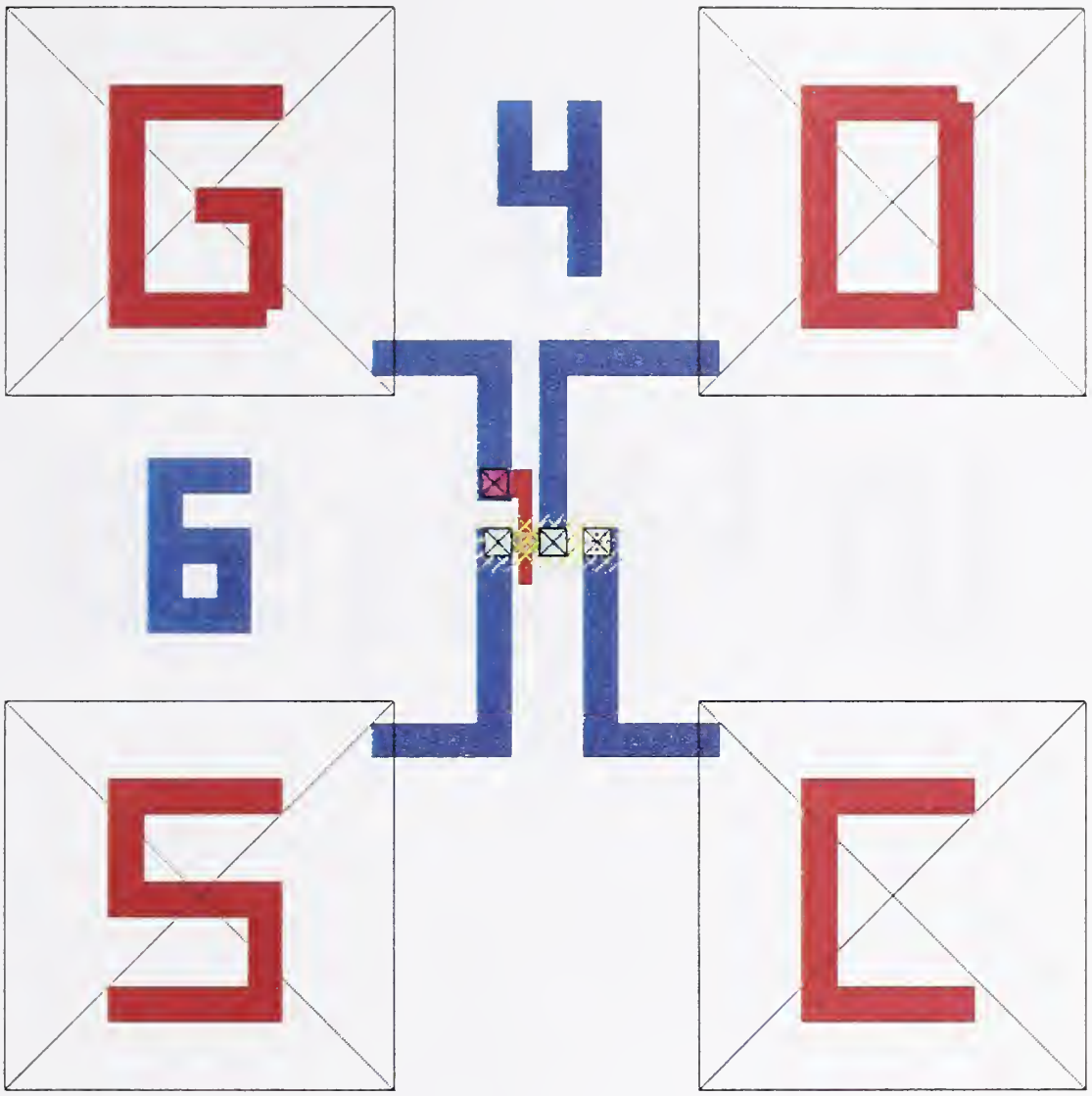

Figure 5. Minimum-sized n-channel MOSFET found in the test library, NIST8, and NIST9.

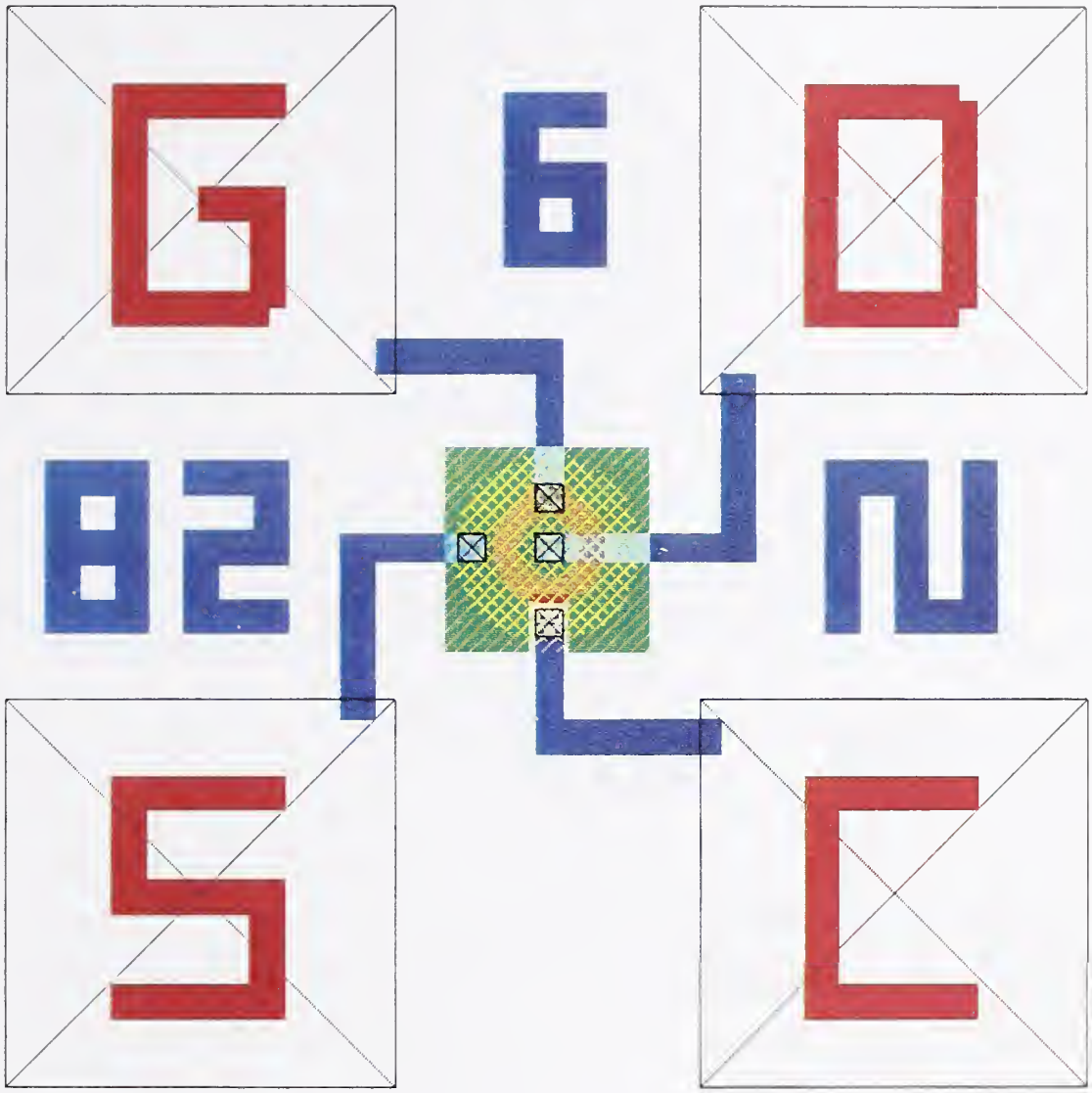

Figure 6. Circular n-channel MOSFET found in the test library, NIST8, and NIST9.

Figure 7. Circular n-channel MOSFET with no channel contact found in the test library, NIST8, and NIST9.

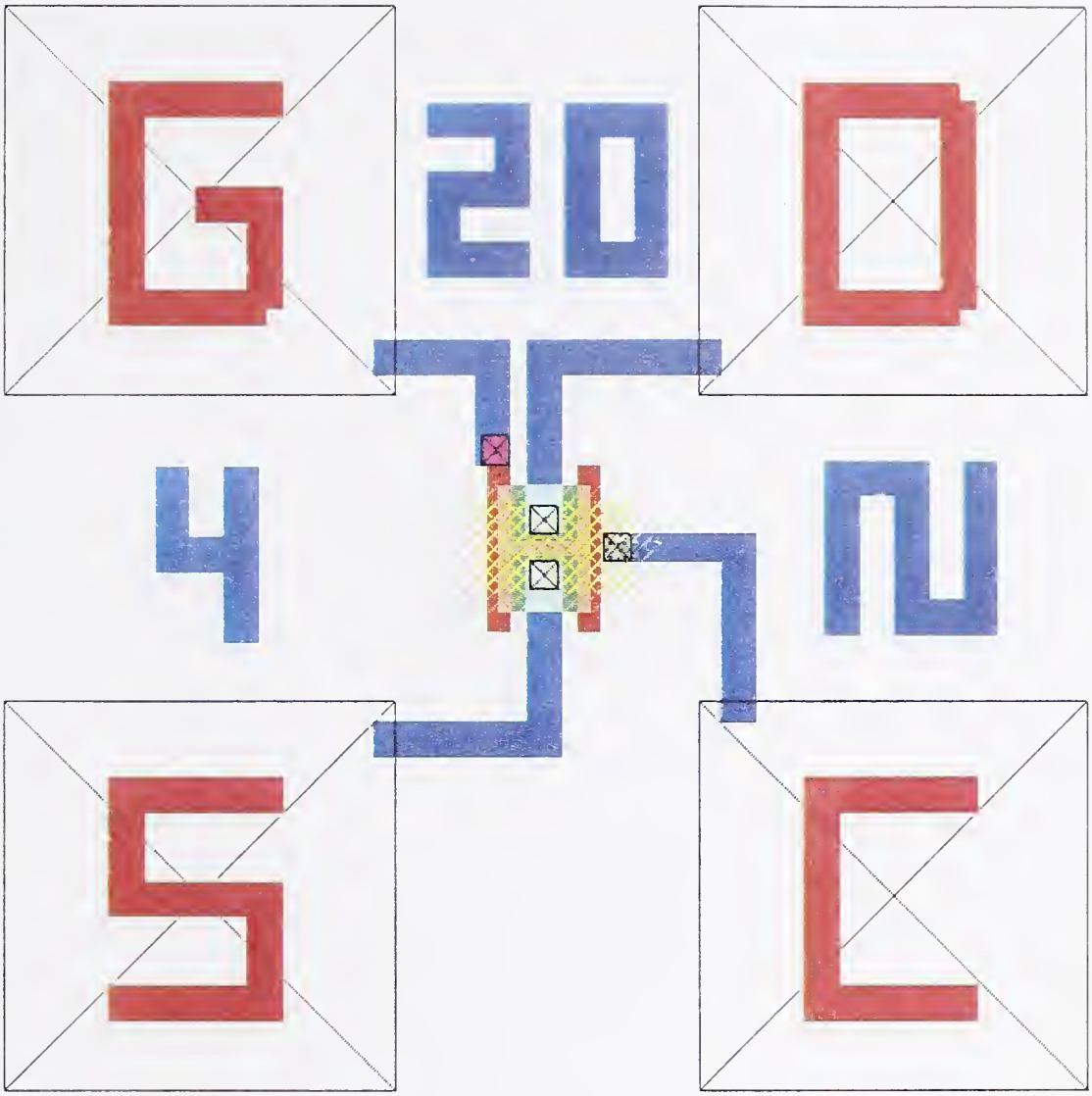

Figure 8. H-gate MOSFET found in the test library, NIST8, and NIST9.

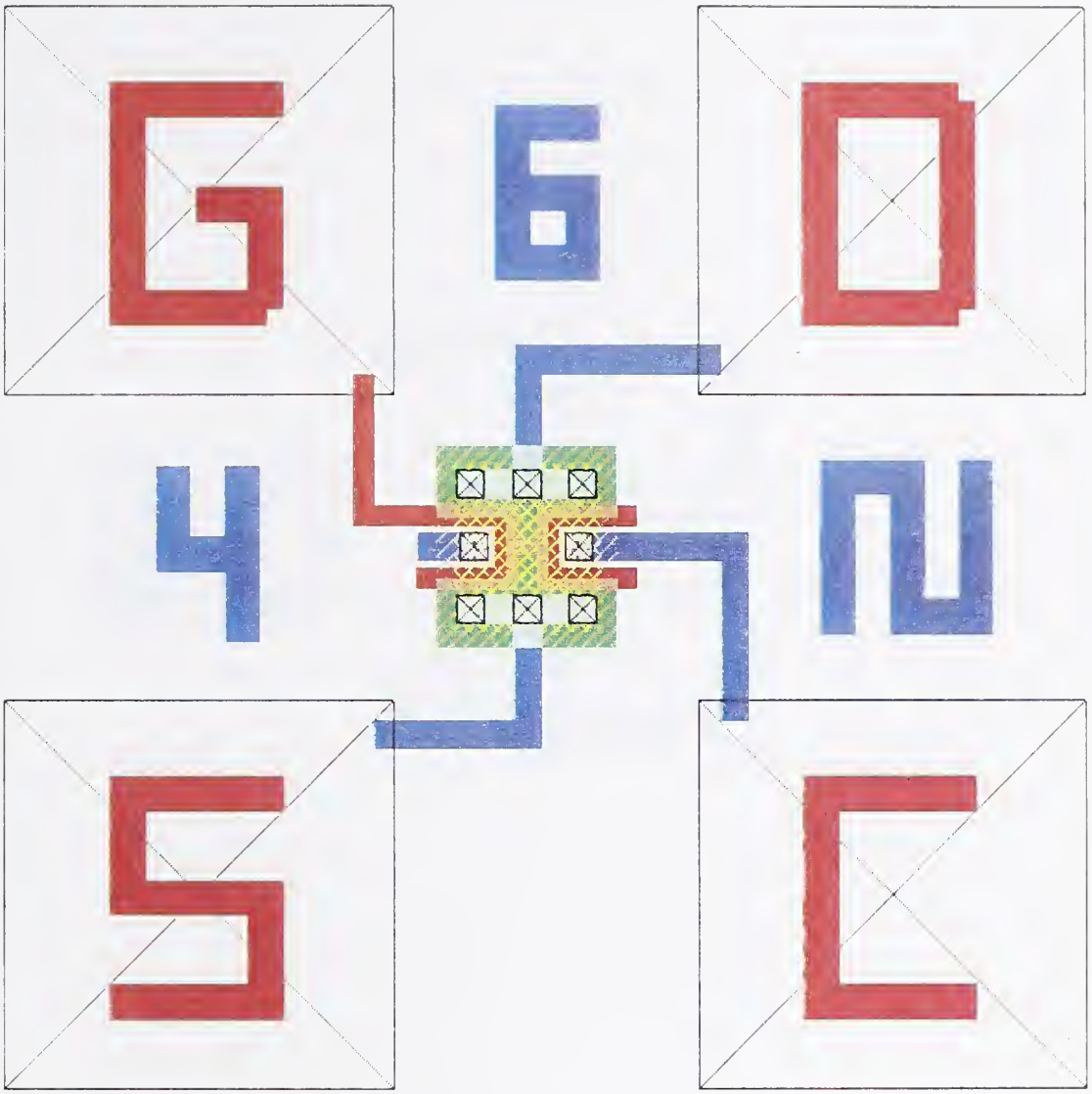

Figure 9. Italic H-gate MOSFET found in the test library, NIST8, and NIST9.

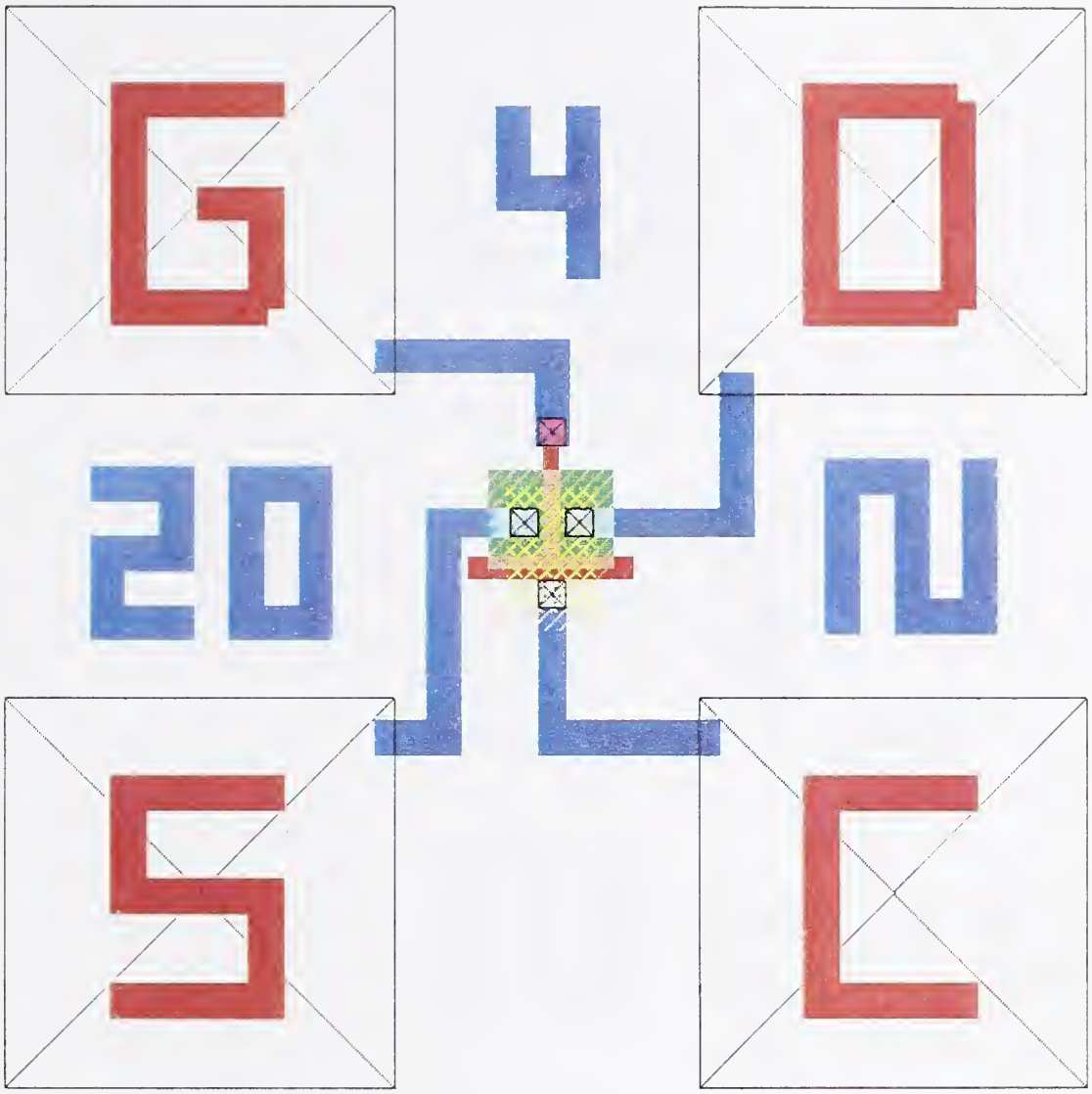

Figure 10. T-gate MOSFET found in the test library, NIST8, and NIST9.

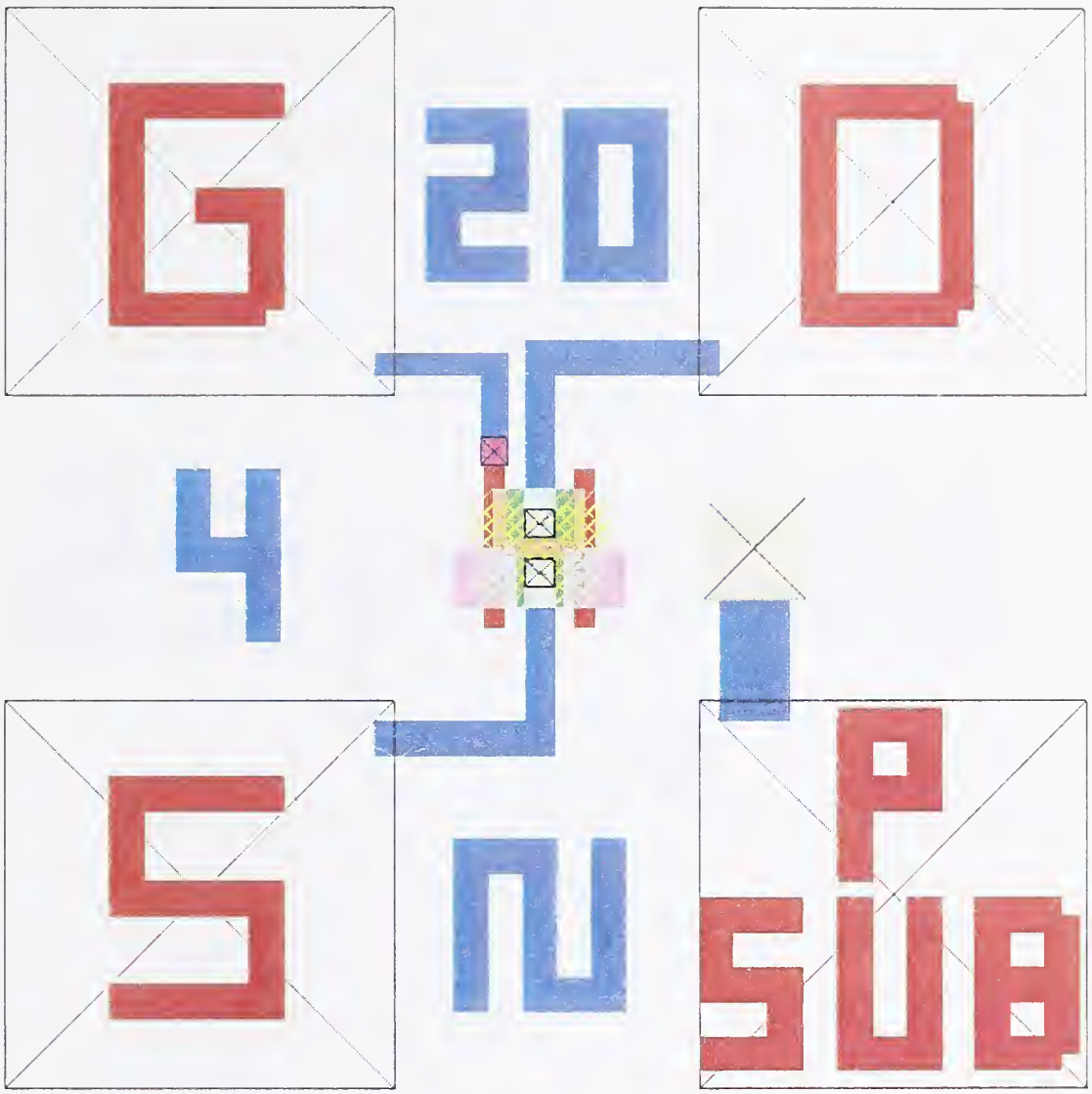

Figure 11. H-gate MOSFET with source-to-channel tie found in the test library, NIST8, and NIST9.

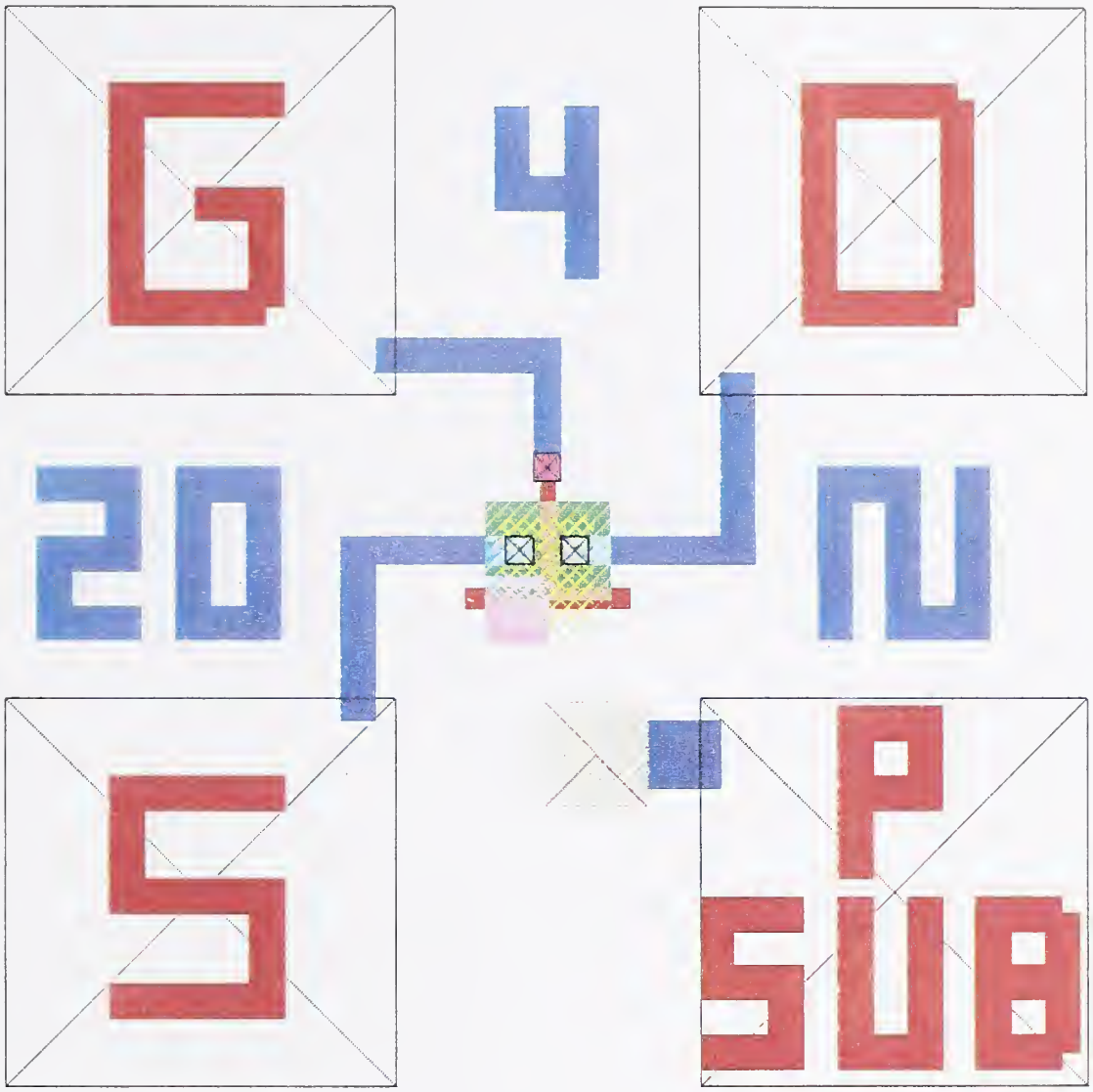

Figure 12. T-gate MOSFET with source-to-channel tie found in the test library, NIST8 and NIST9.

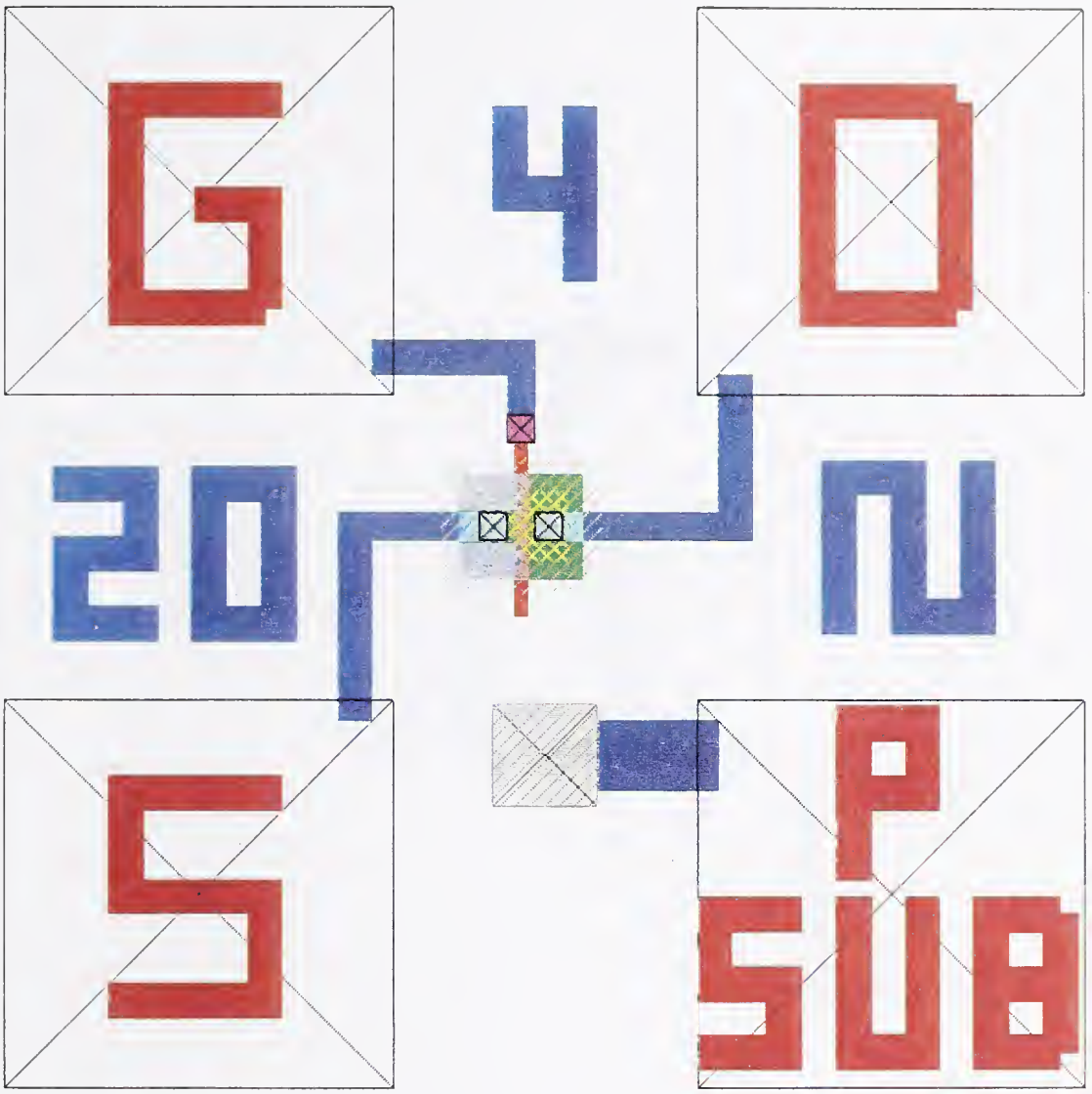

Figure 13. *N*-channel MOSFET with source-to-channel tie found in the test library and NIST9.

Figure 14. *N*-channel depletion-mode MOSFET found in the test library and NIST9.

Figure 15. First bipolar design (*npn*) on NIST9 with the base contact beside the emitter and with a full implant.

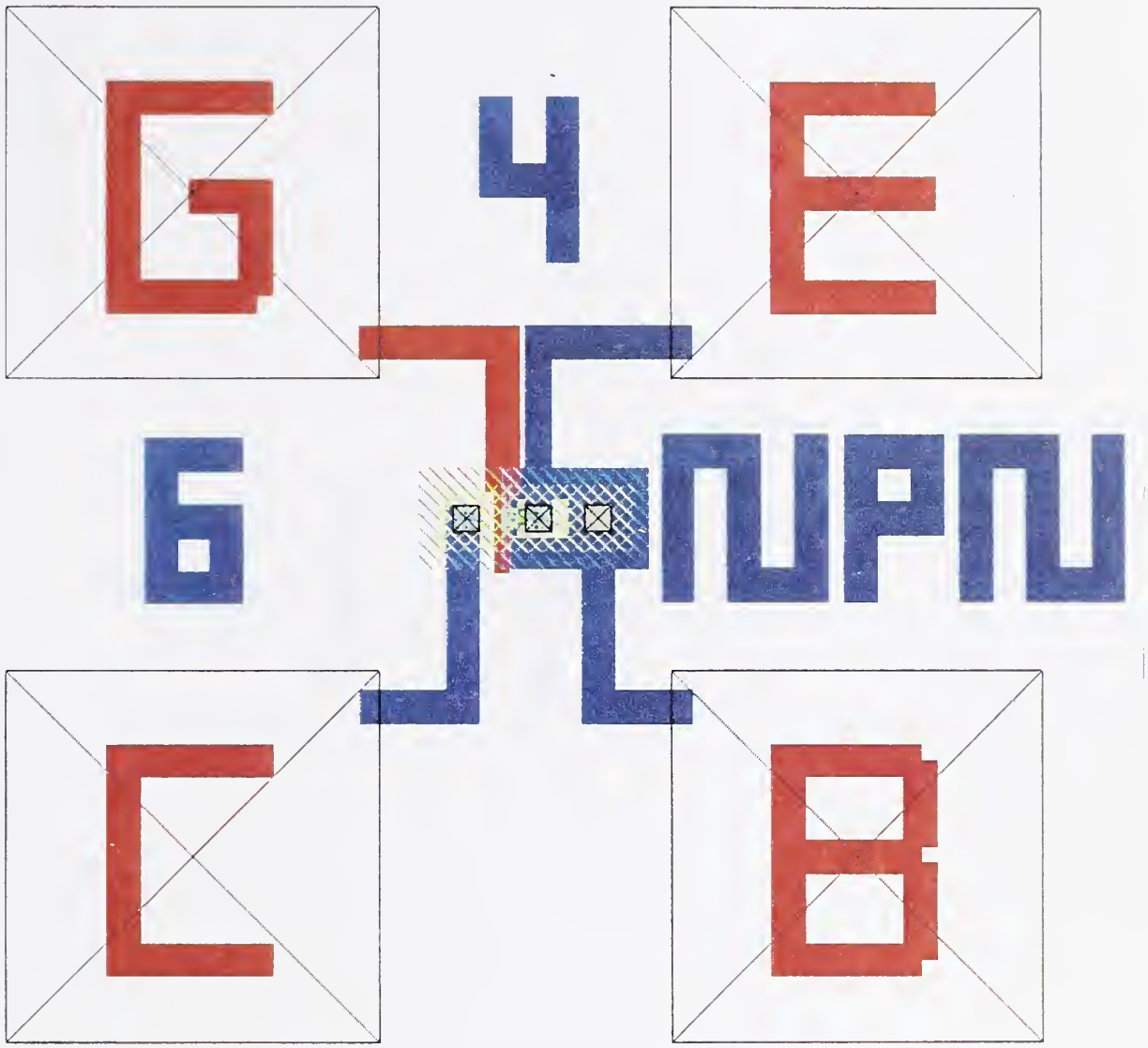

Figure 16. Second bipolar design (*npn*) on NIST9 with the base contact beside the emitter and with a half implant.

Figure 17. Third bipolar design (*npn*) on NIST9 with the base contact below the gate and with a full implant.

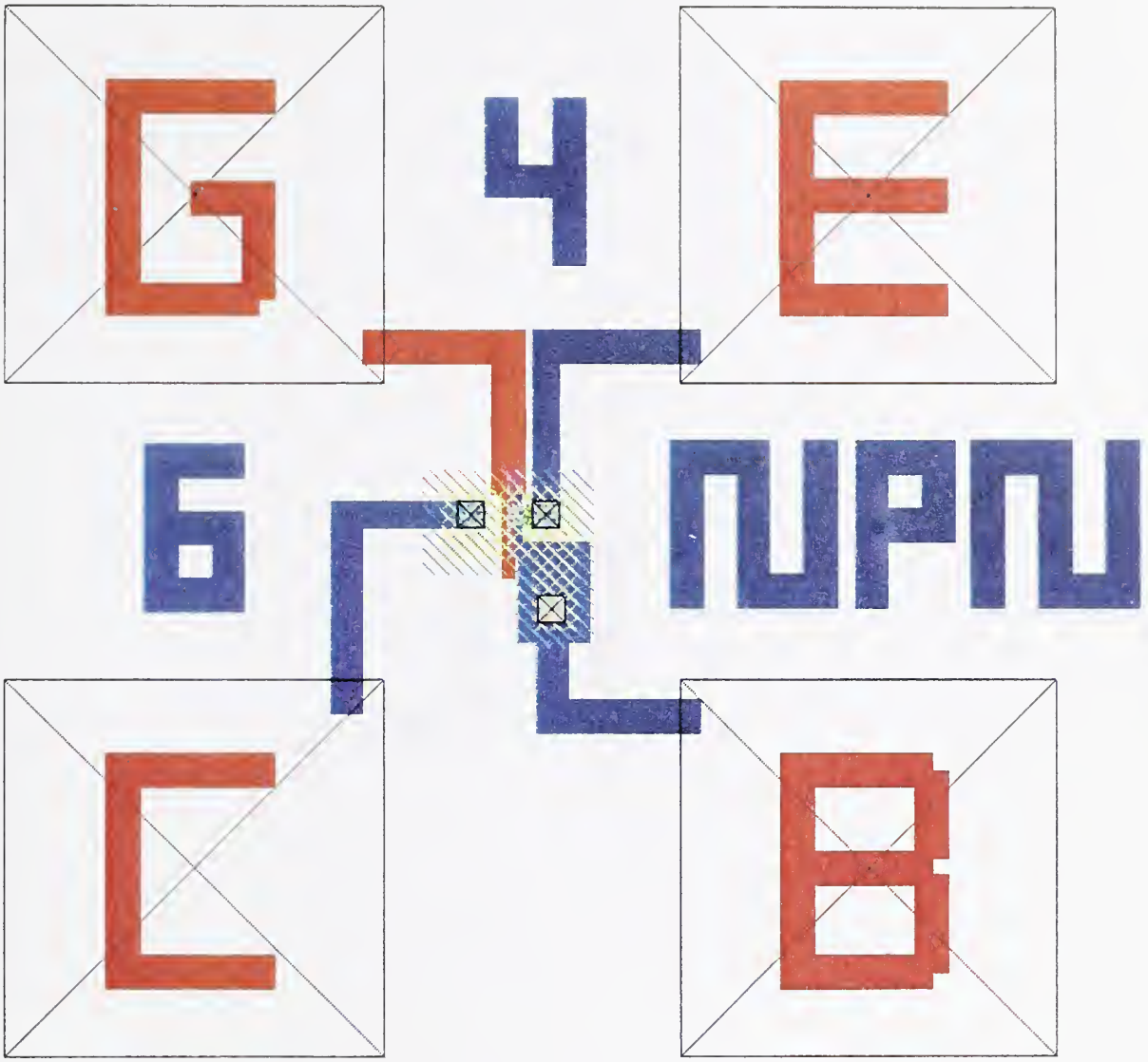

Figure 18. Fourth bipolar design (*npn*) on NIST9 with the base contact below the gate and with a half implant.

Figure 19. Fifth bipolar design (*npn*) on NIST9 with an *n*-channel MOSFET gate connected to its base.

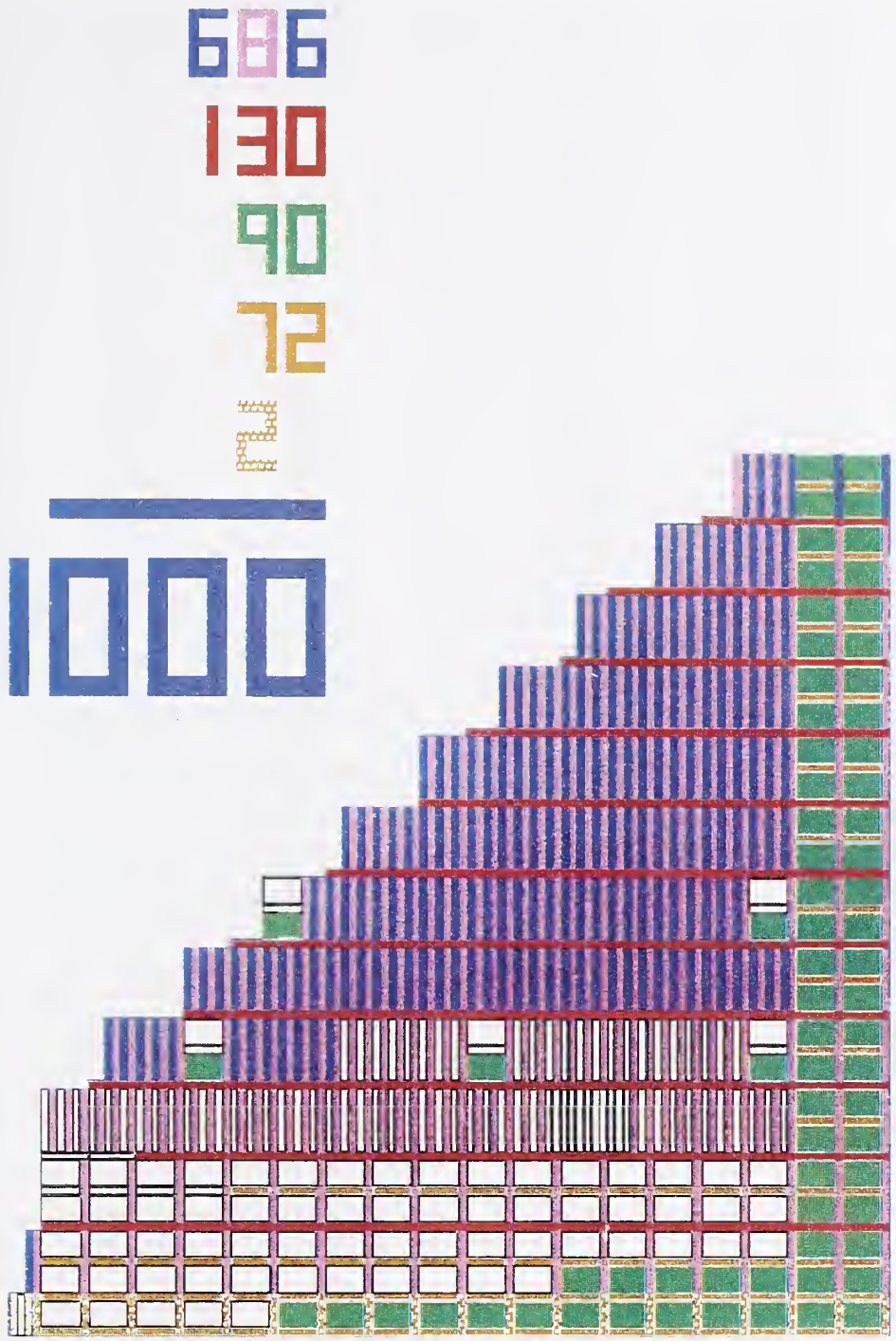

Figure 20. Cell structure of the test library with module count.

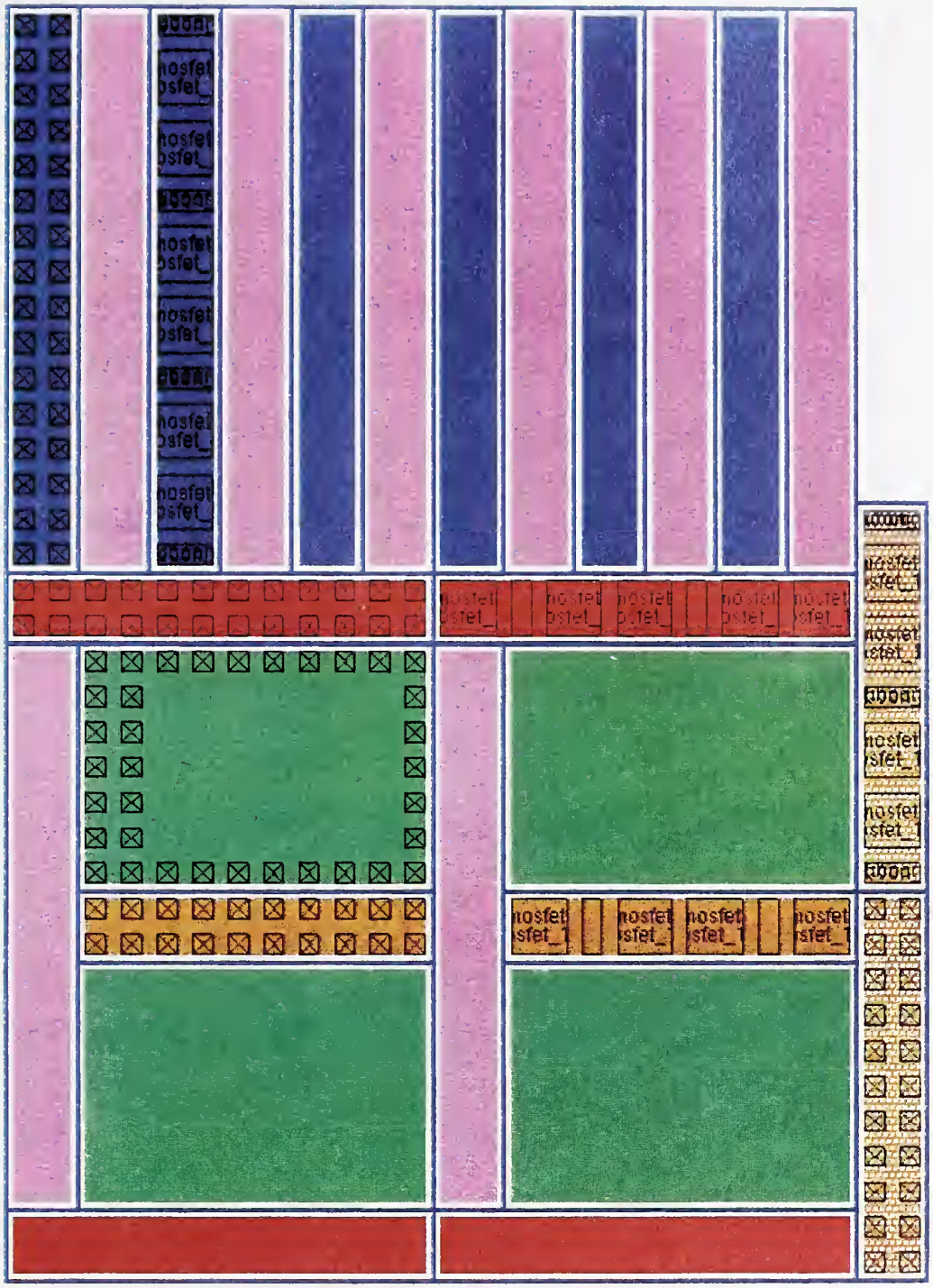

Figure 21. Module spacings used in the test library, NIST8, and NIST9.

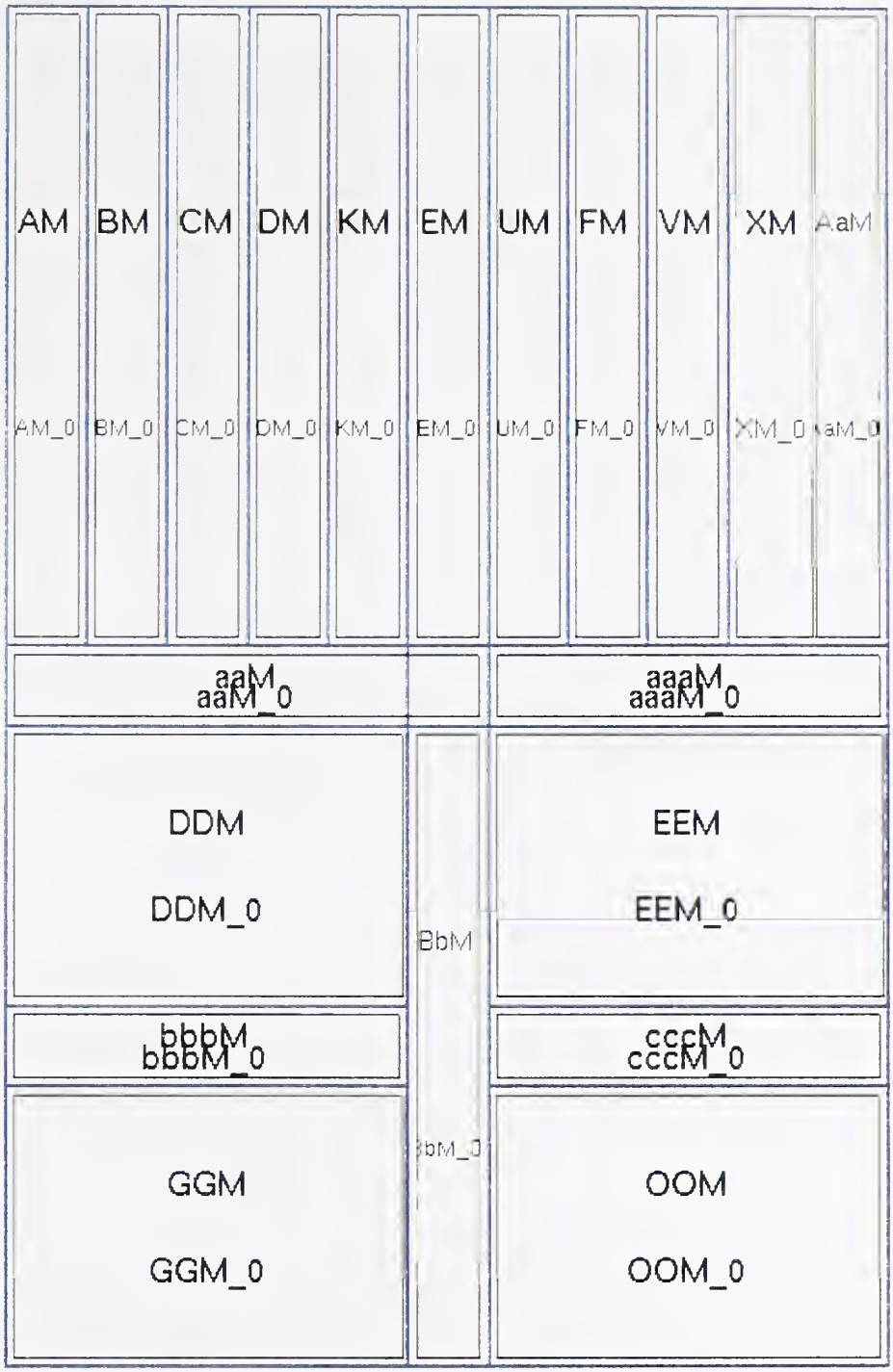

Figure 22. Cell structure of NIST8.

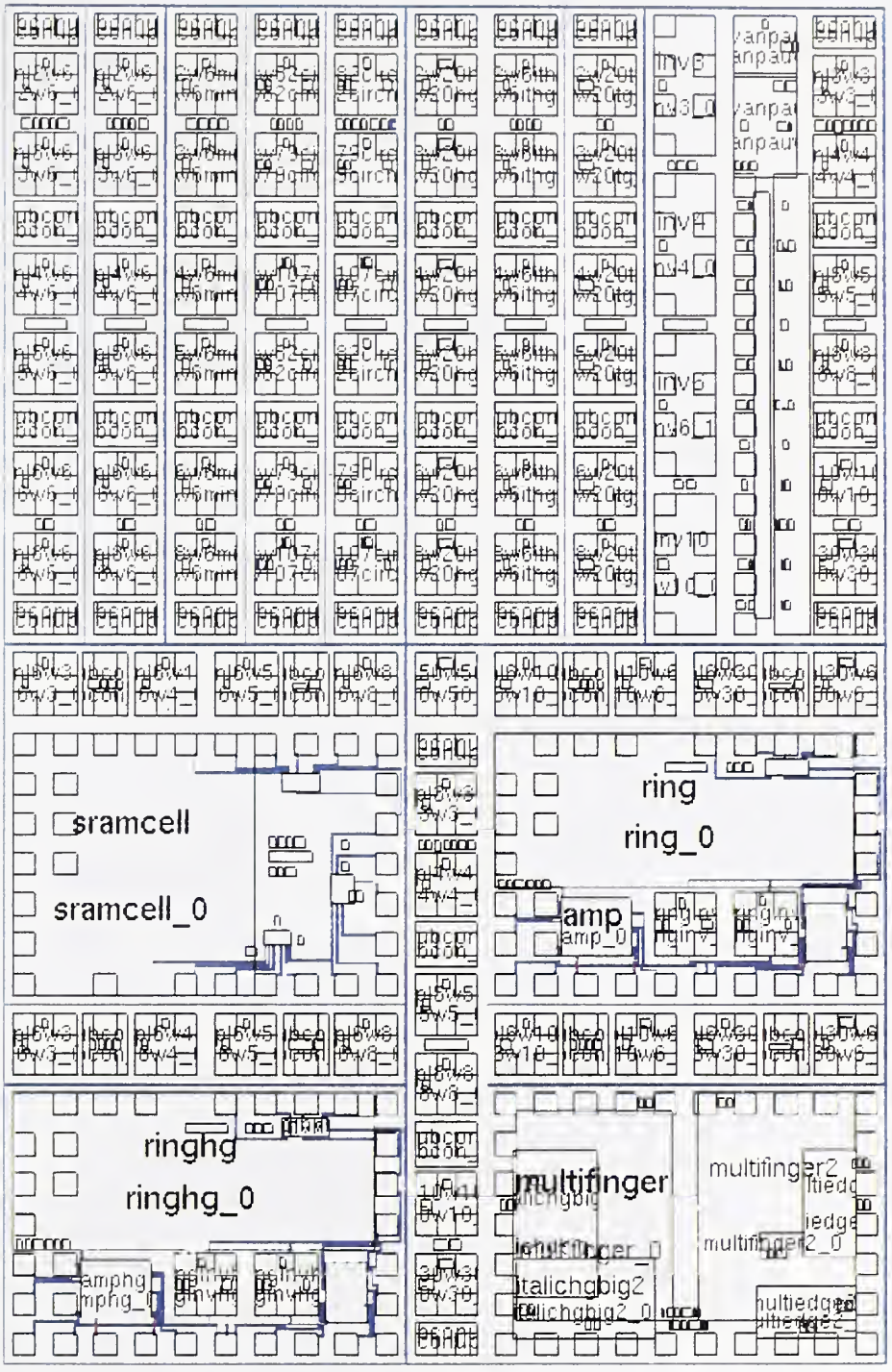

Figure 23. Subcell structure of NIST8.

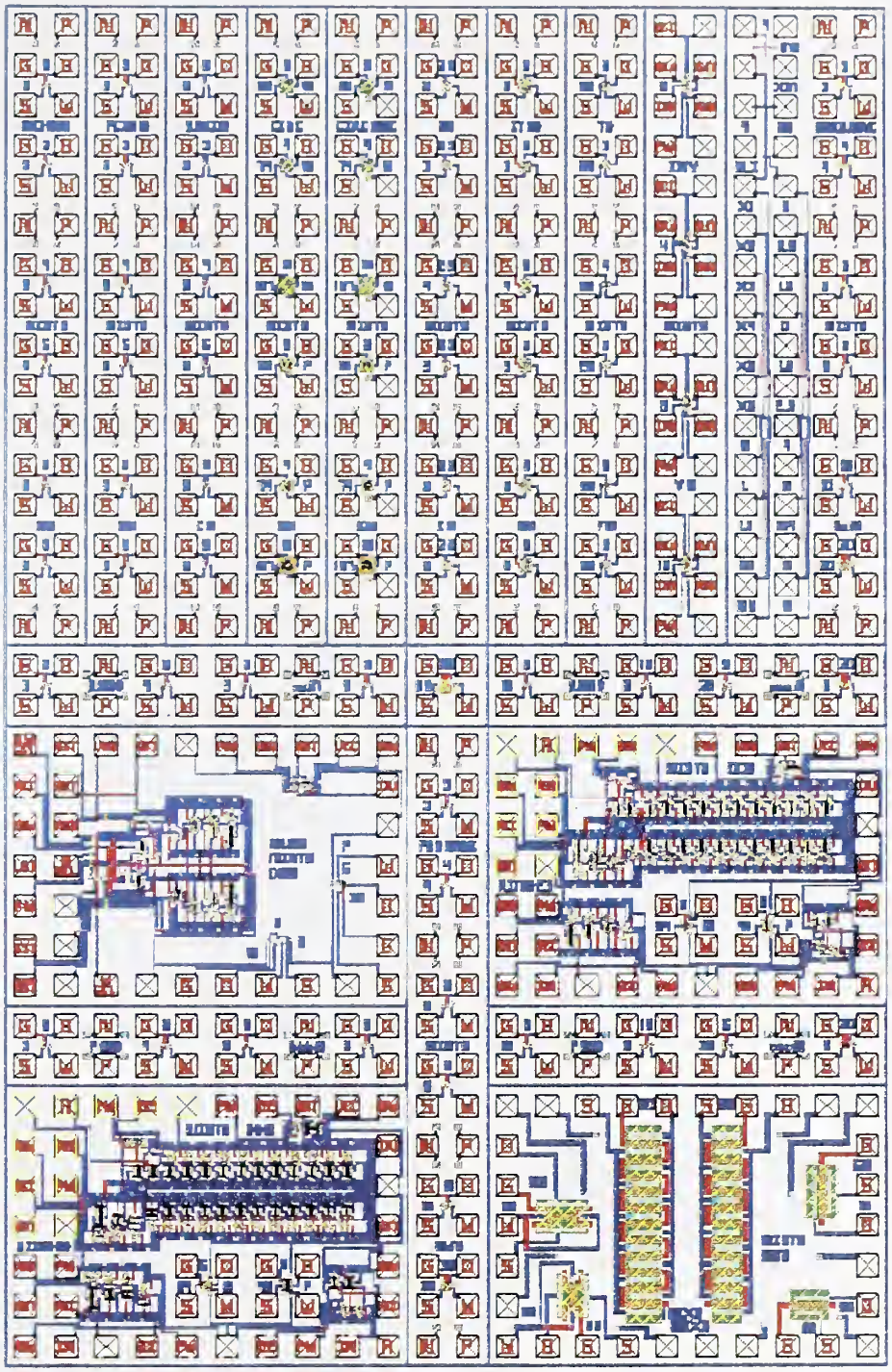

Figure 24. CMOS Test Chip, NIST8.

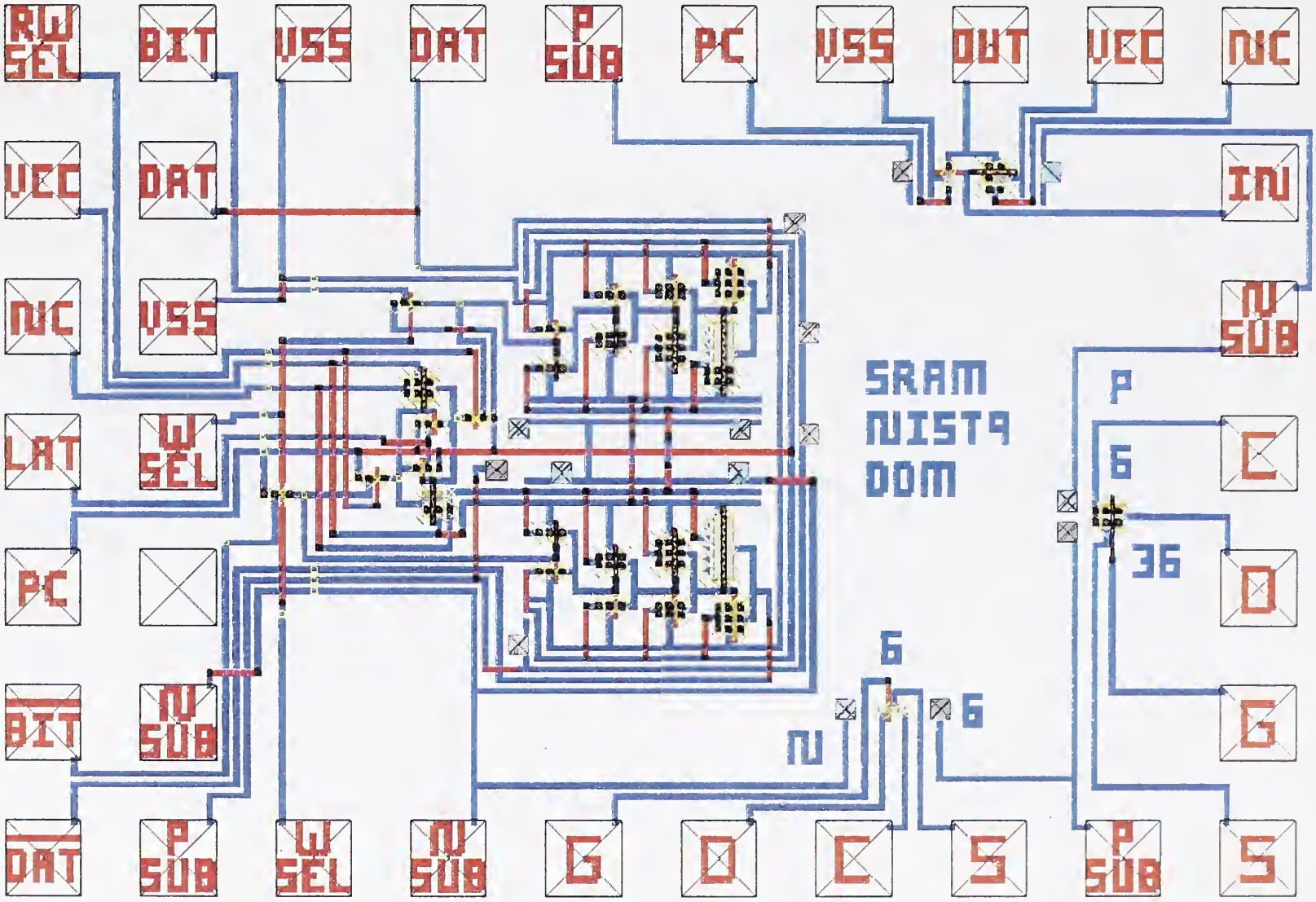

Figure 25. Static RAM module DDM found in the test library, NIST8, and NIST9.

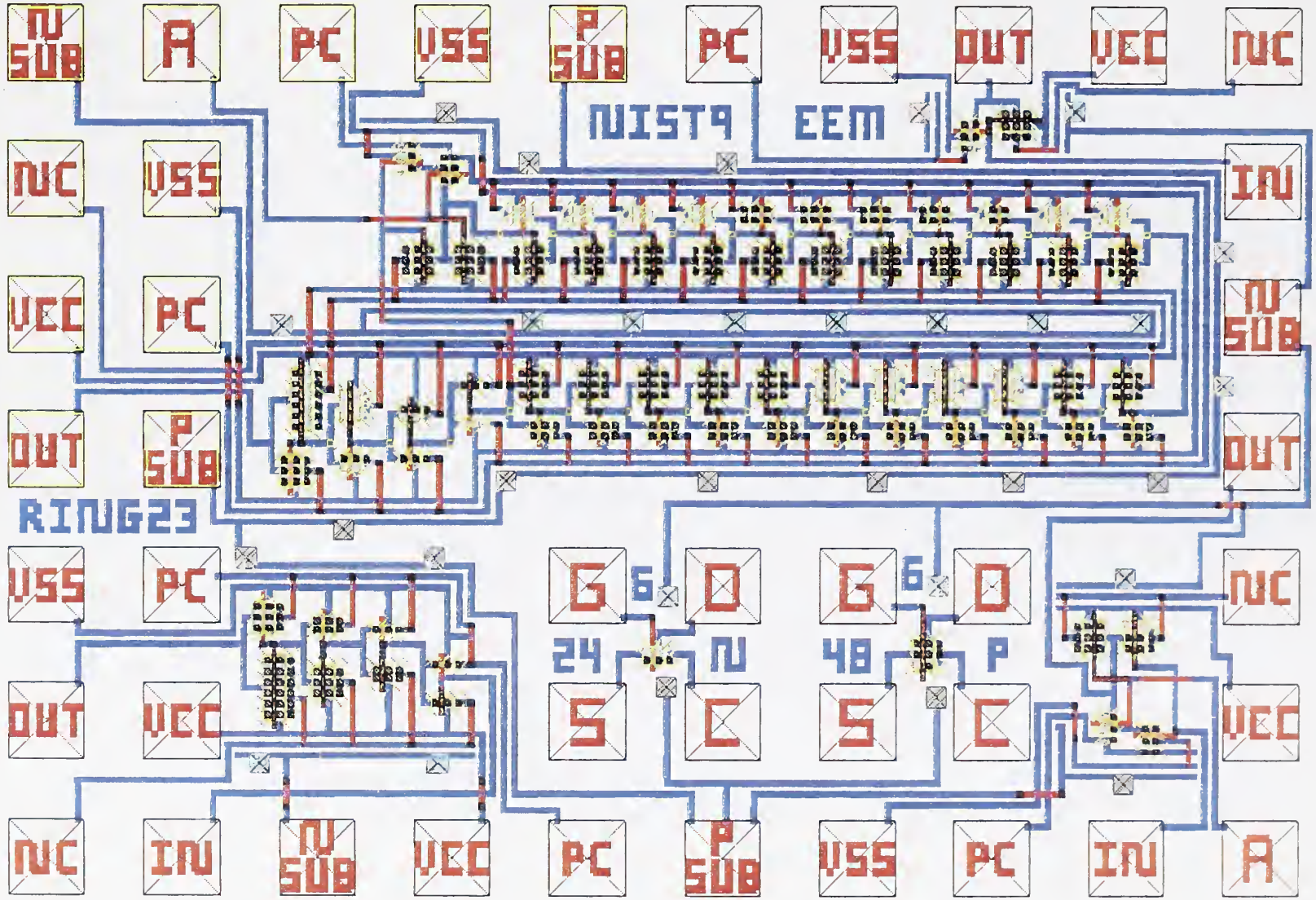

Figure 26. Ring oscillator module EEM found in the test library, NIST8, and NIST9.

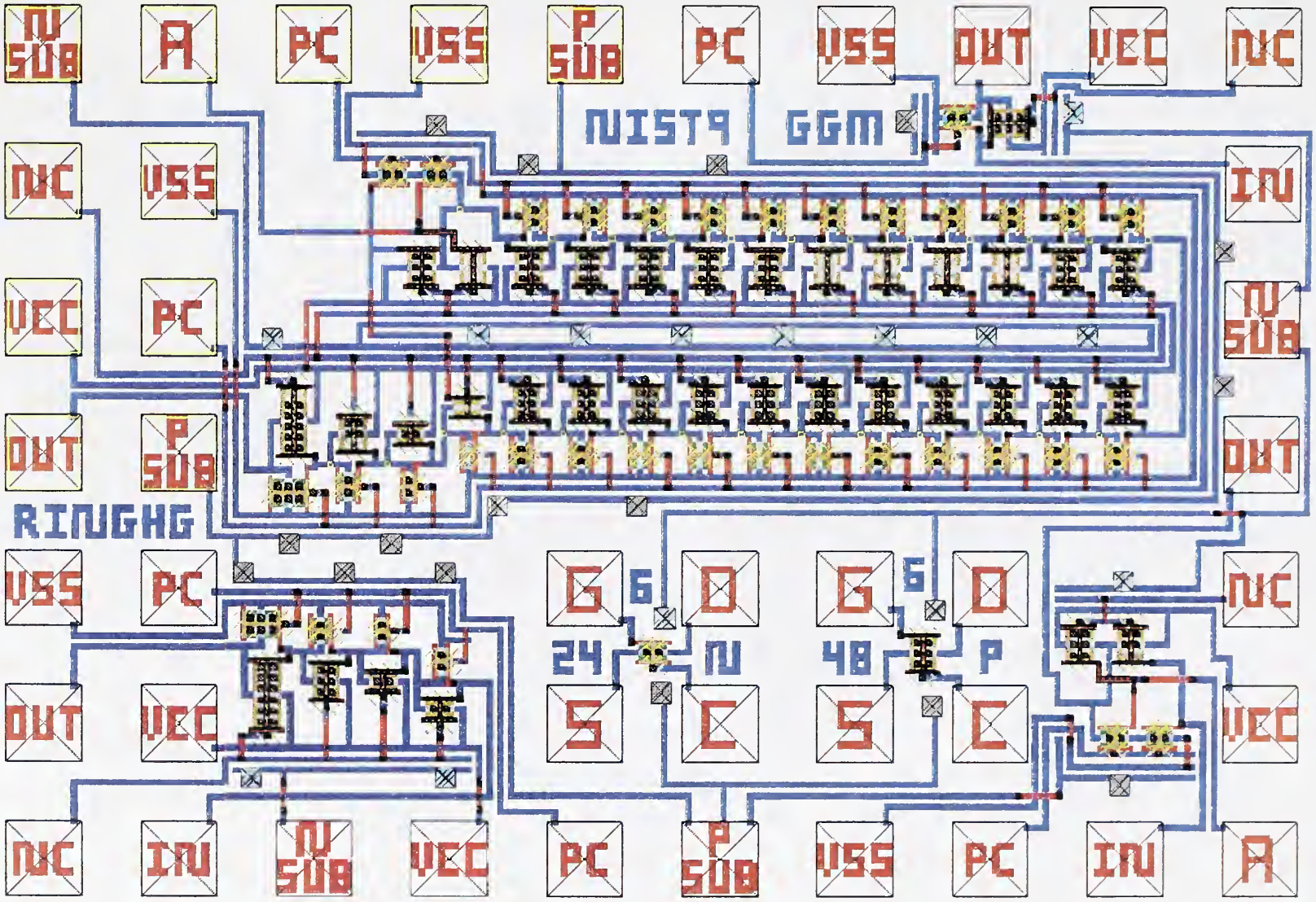

Figure 27. H-gate MOSFET ring oscillator module GGM found in the test library, NIST8, and NIST9.

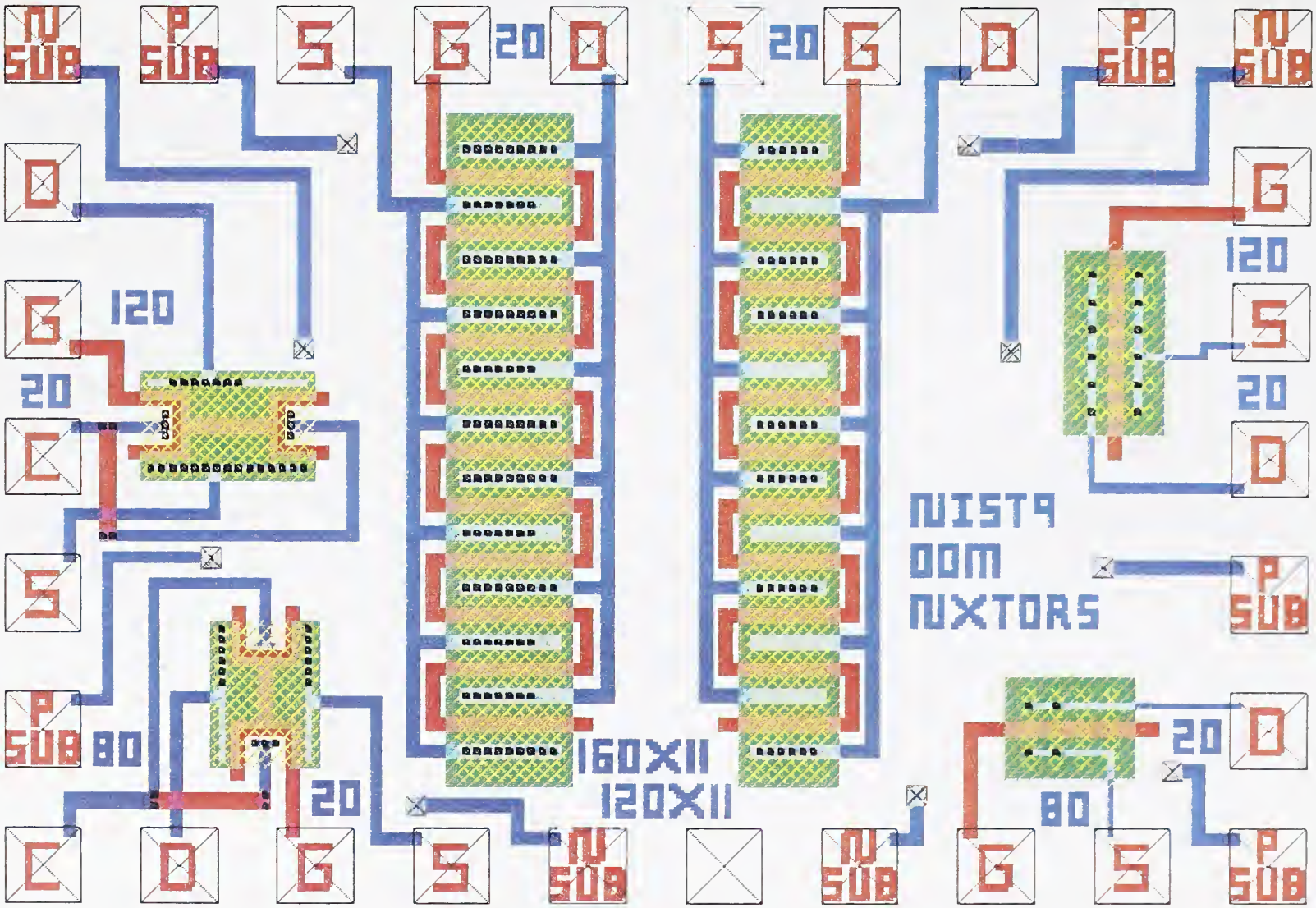

Figure 28. Large n-channel MOSFETs for radiation investigations (module OOM) found in the test library, NIST8, and NIST9.

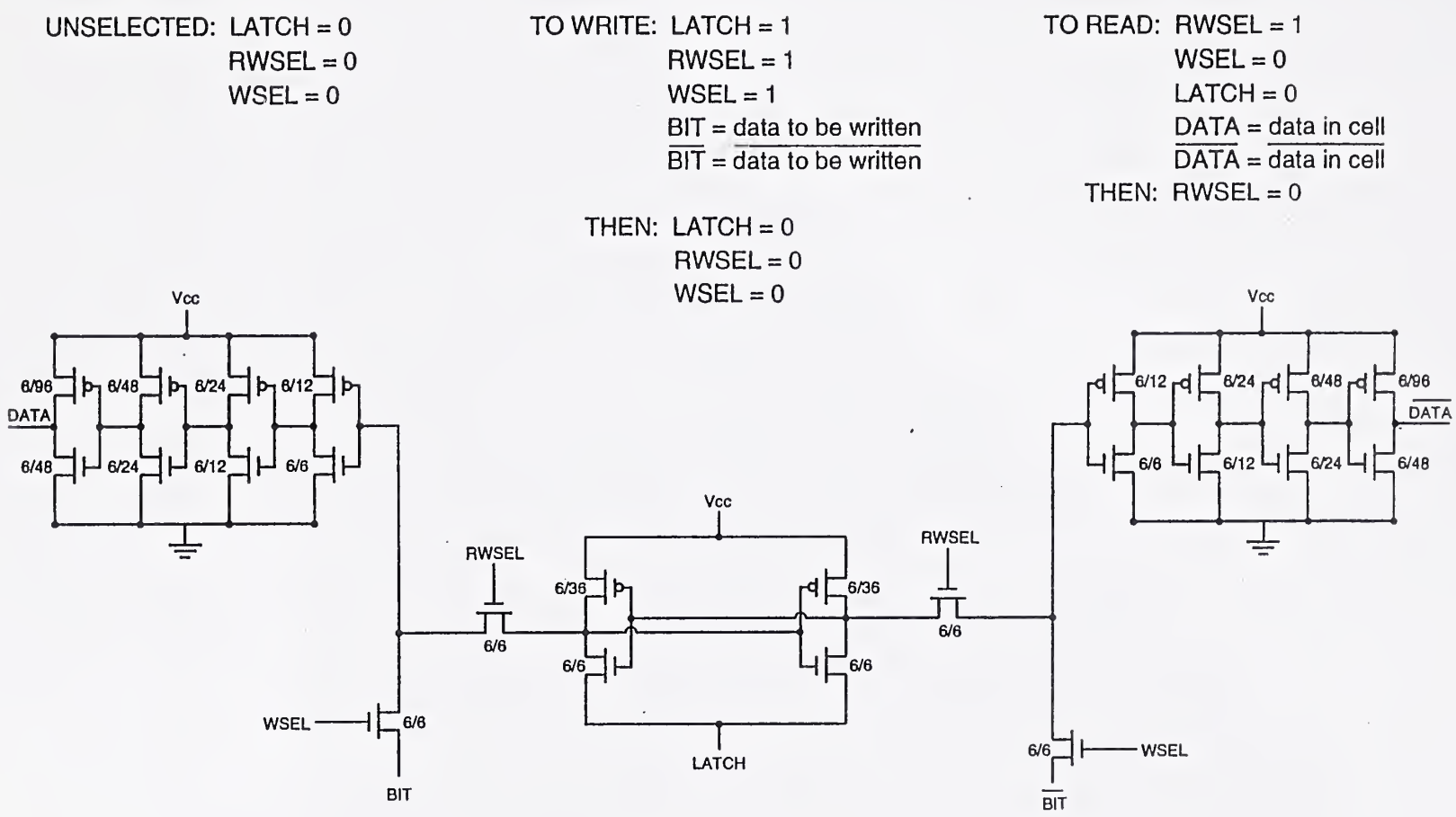

Figure 29. Circuit diagram of the static RAM cell (and how to test it).

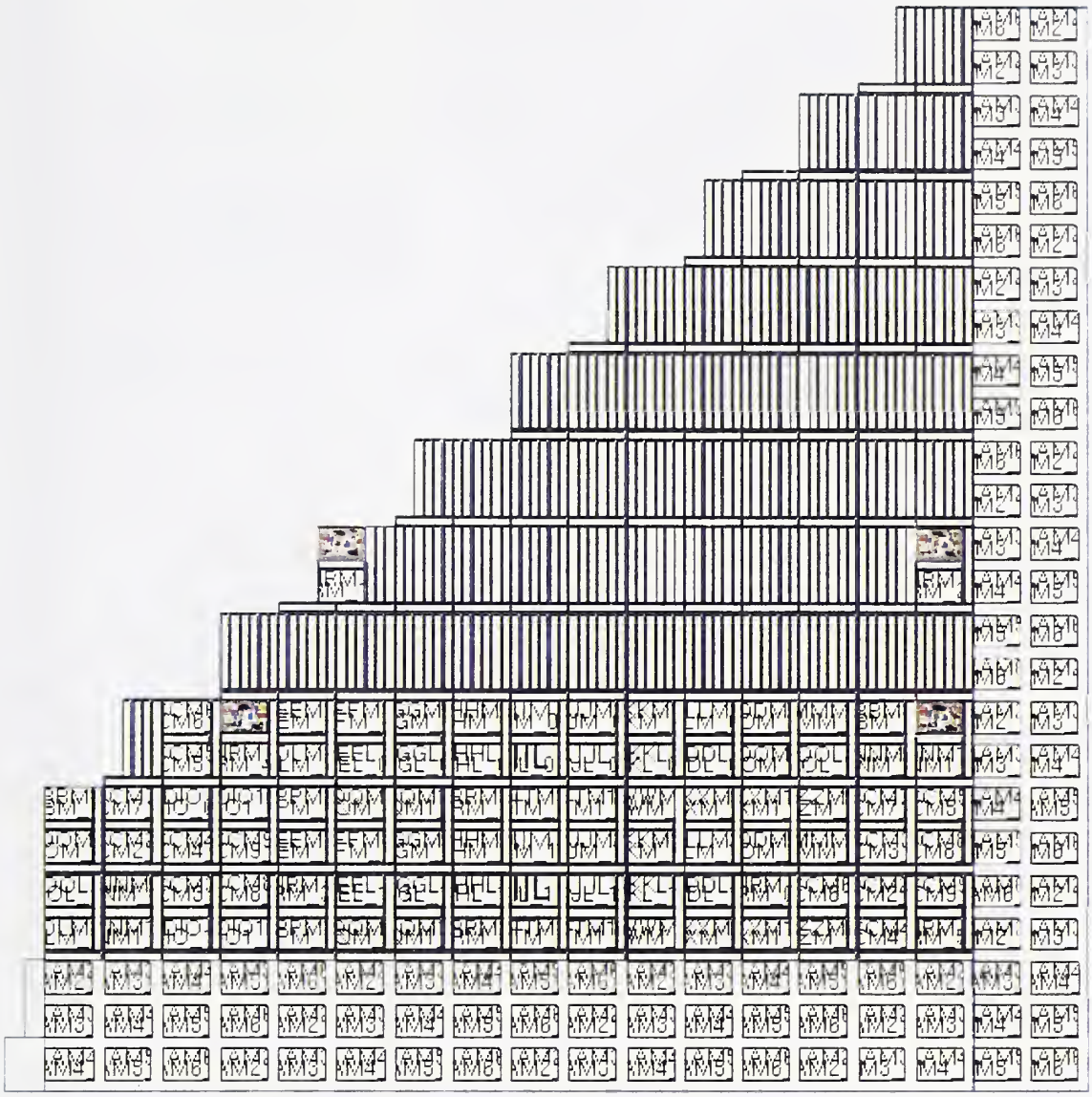

Figure 30. Cell structure of the SOI/SIMOX test wafer NIST9.

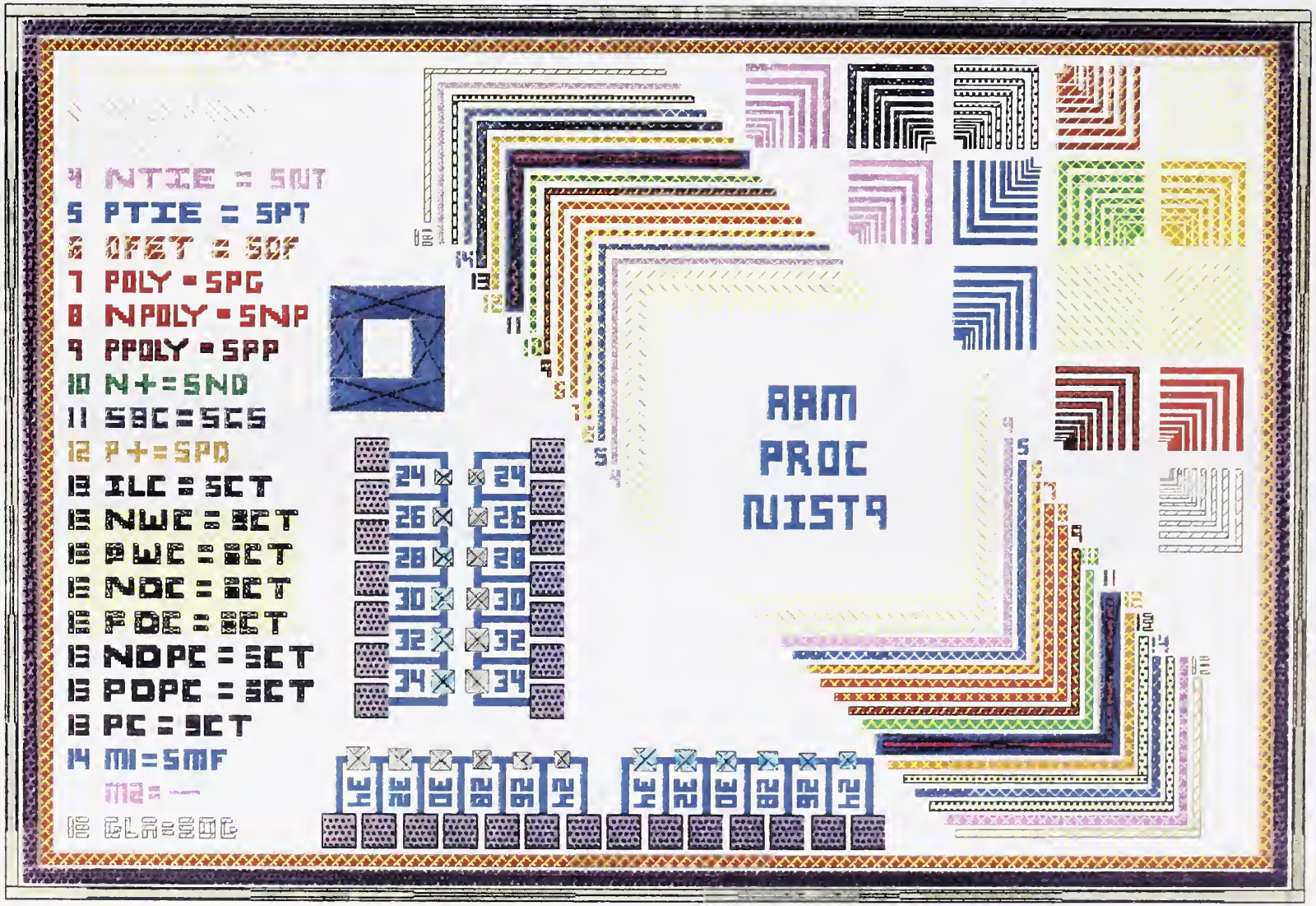

Figure 31. Processing module AAM found in the test library and NIST9.

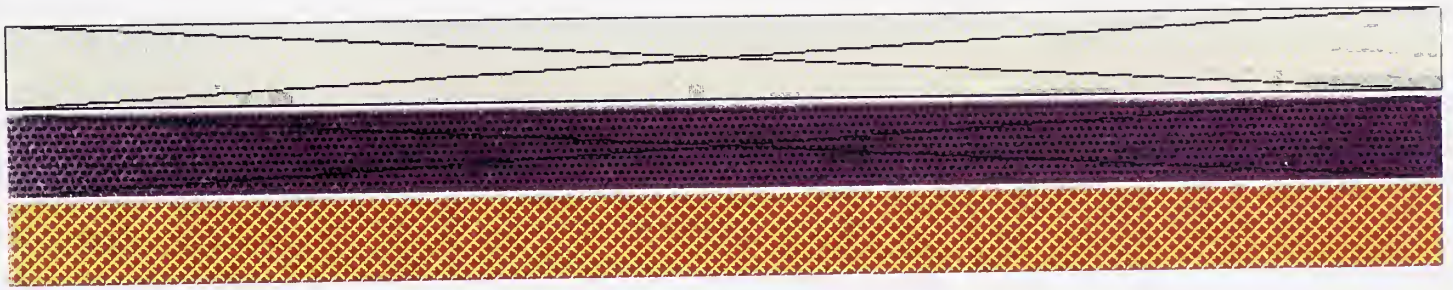

Figure 32. Processing module AAM1 found in the test library and NIST9.

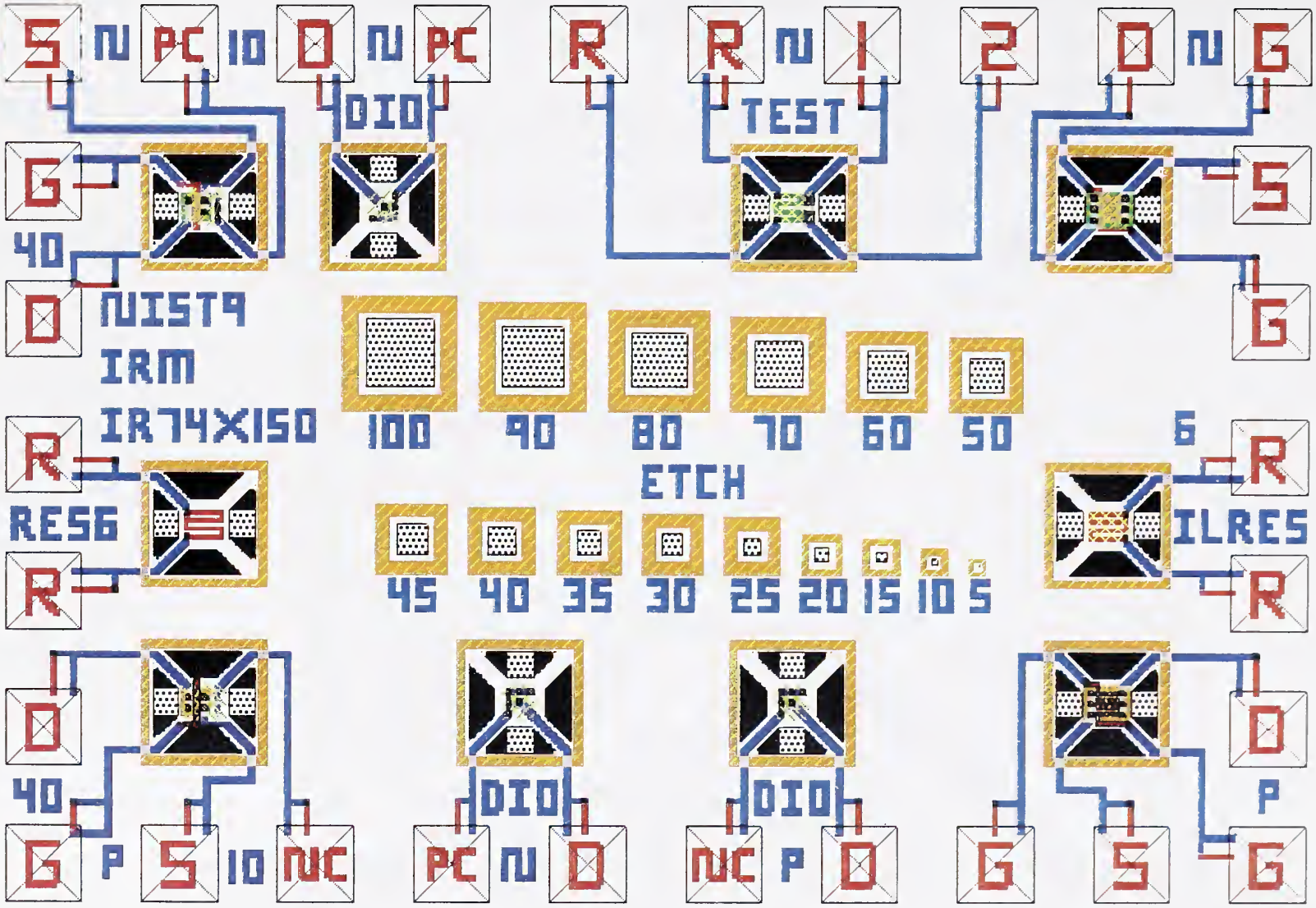

Figure 33. Micromachining module IRM found in the test library and NIST9.

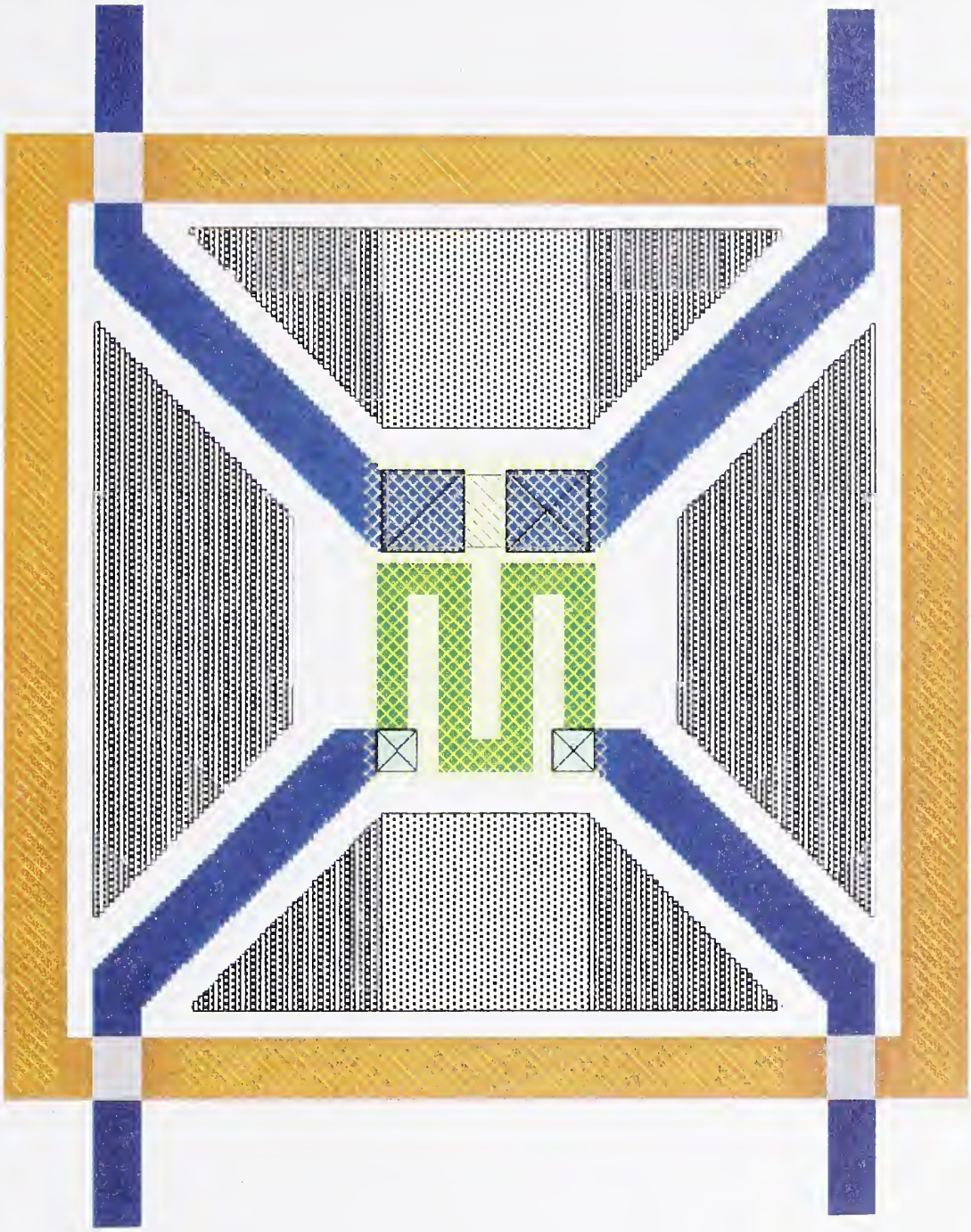

Figure 34. OH breath analyzer.